JIEE Časopis priemyselnej elektrotechniky
Journal of Industrial Electrical Engineering
ISSN 2454-0900
www.jiee.eu

Application of analog multiplier in industrial electrical engineering

[1]*Milan ĎAĎOVSKÝ*, [2]*Irena KOVÁČOVÁ*

[1,2] Department of Theoretical and Industrial Electrical Engineering, Faculty of Electrical Engineering and Informatics, Technical University of Košice, Slovak Republic

[1]milan.dadovsky@student.tuke.sk, [2]irena.kovacova@tuke.sk

***Abstract* — The paper deals with application of analog multiplier in electrical engineering. First, it consists of theoretical information about analog multipliers. There are mentioned main principles and features of analog multipliers, e.g. multiplier errors. Mainly, the document gives description of used analog multiplier in integrated form called AD633J. Next part of paper consists of AD633J time domain simulation model creation in OrCad Pspice and its practical measurements, both compared.**

***Keywords* — analog, errors, measurement, multiplier, model, OrCad, Pspice, simulation, waveform**

I. Introduction

Analog multipliers can be made of discrete components. Nowadays there are many companies producing easier form of analog multipliers - integrated circuits. World-known companies such as Analog Devices and Texas Instruments produce multipliers in various packages to match your expectations.

II. Theory Of Multiplying

A. *What is analog multiplier?*

An analog multiplier is a electronic device that produces an output voltage or current that is proportional to the product of two or more independent input voltages or currents [1]. In addition to multiplying and dividing, multipliers can perform other mathematical functions: squaring, square-rooting, logarithm and modulation functions. The most applications include processes where a real-time response is required. Analog multiplier circuit symbol is showed in Fig.1.

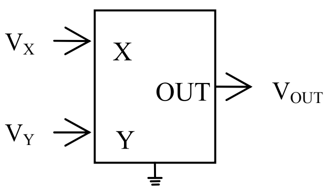


Fig. 1 Circuit symbol of analog multiplier

The general form of the ideal multiplier transfer function is:

$$V_{out} = \frac{1}{k}.V_x.V_Y \qquad (1)$$

, where $V_{out}$is output voltage in volts, V_X is input voltage applied to X input, V_Y is input voltage applied to Y input, k is constant (usually 10V).

If constant k is 10 then (1) becomes:

$$V_{out} = \frac{V_x . V_Y}{10} \quad (2)$$

Multipliers are always designed to have a dimensional constant k in the value of 10, so either input can have any value in the 10V range without causing the output to exceed 10V. For applications in which the maximum range of the inputs is less than 10V it is better to use smaller value of k. Many multipliers have an option to adjust dimensional constant with external components connected to appropriate pins of integrated circuit.

B. Classification of analog multipliers

Analog multipliers are classified according to the number of quadrants in which they can operate. The quadrants are the four quadrants of the Cartesian coordinate system as you can see in Fig. 2 [2].

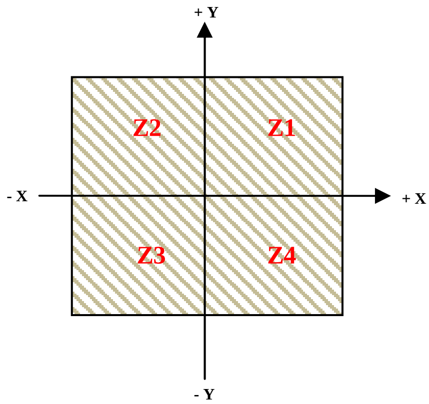


Fig. 2 Operational quadrants of analog multiplier

Classification:

1. One-quadrant multipliers - all input signals and output signal have the same polarity (Z1 in Fig. 2).
2. Two-quadrant multipliers - one of input signals must be one-polarity and the other can be of both polarities. Output signal can be either positive or negative (Z1 and Z2 in Fig. 2).
3. Four-quadrant multipliers - allow operation with all input and output signal polarities (all Zx in Fig. 2).

C. Basic terms and multiplying errors

The most important specification is accuracy of the multiplier which is defined as total error of the multiplier at room temperature and nominal supply voltage.

The scale-factor error is the percentages expressed difference between the average scale factor and the ideal scale factor that is 10V.

Output offset of output-amplifier stage is usually minimized at manufacturing process.

Dynamic parameters include signal bandwidth, full-power response, slew rate, small-signal amplitude error, and settling time.

Equation (1) representing transfer function of ideal analog multiplier becomes more difficult when we are using real device [3]:

$$W = (k + \Delta k).\{(V_X + X_{offset}).(V_Y + Y_{offset}) + Z_{offset} + f(X,Y)\} \quad (3)$$

where k is Multiplier Scale Factor, Δk is Scale Factor Error, V_X is X-Input Signal, X_{offset} is X-Input Offset Voltage, V_Y is Y-Input Signal, Y_{offset} is Y-Input Offset Voltage, Z_{offset} is Multiplier Output Offset Voltage, $f(X, Y)$ is Nonlinearity.

III. AD633- Precision Analog Multiplier

In the market there are many types of analog multipliers. In the Table 1 you can see comparison of some available analog multipliers made by Analog Devices company [4]. We chose to analyze AD633 integrated circuit [5].

Table 1
Comparison of Available Analog Multipliers

Part #	Transfer Function	Vin Range (V)	Bandwidth -3 dB (Hz)	Slew Rate (V/µs)	Settling Time to 0.1%	Total Error (%)	Vout Range (V)	Isupply (A)
AD835	[(X1-X2)(Y1-Y2)/U] + Z	±1	250M	1k	20	0,3	±2.5 V	25m
AD633	[(X1-X2)(Y1-Y2)/10] + Z	±10	1M	20	2	2	±11 V	6m
AD734	[(X1-X2)(Y1-Y2)/(U1-U2)] + (Z1-Z2)	±12.5	10M	450	200	0,4	12 V	12m
AD834	(4 mA)(XY)	±1	500M	-	-	2	±4.04 mA	35m
AD538	[y(z/x)]^m	±10	400k	1,4	-	1	±11 V	7m
AD539	-(vx*vy)/vu	±4.2	25M	-	-	2,5	±2.8 mA	10.2m
AD632	[(X1-X2)(Y1-Y2)/10] + Z2	±12	1M	20	2	0,5	±11 V	6m
AD534	[(X1-X2)(Y1-Y2)/10 V] + Z2	±10	1M	20	2	0,25	±11 V	6m
AD532	(X1-X2)(Y1-Y2)/10 V	±10	1M	45	-	1	±10 V	6m

AD633 is four-quadrant multiplier which includes high impedance differential inputs (X1, X2, Y1, Y2), and a high impedance summing input (Z). Transfer function of AD633 is:

$$V_{out} = \frac{(X_1 - X_2).(Y_1 - Y_2)}{10} + Z \qquad (4)$$

The versatility of the AD633 is not compromised by its simple construction. The AD633 is laser calibrated which guarantee total accuracy of 2% of full scale. Block diagram of AD633 is shown in Fig. 3.

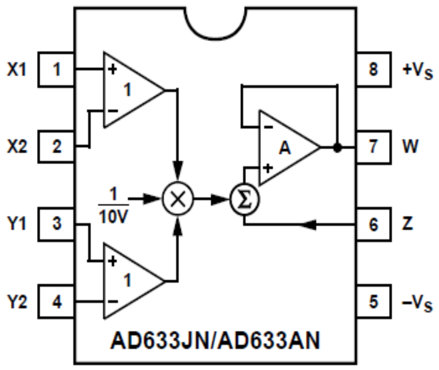


Fig. 3 Block diagram of AD633

The AD633 is available in 8-lead PDIP and SOIC packages. J grade is suitable to operate over the 0°C to 70°C and A grade from −40°C to +85°C. Selected specifications of AD633 are shown in the Table 2 below.

Table 2
Selected Specifications of AD633, $T_A = 25°C$, $V_S = \pm15V$, $R_L \geq 2k\Omega$

Parameter	Value
Total error	±2% of full scale
Scale voltage error	±0,25% full scale
Frequency bandwidth	1MHz
Quiescent current	4mA
Output density	0,8µV/√Hz
Recommended supply voltage	±15V
Slew rate	20V/µs
Short circuit current	30mA
Input signal voltage range	±10V
Settling time at ΔU_O=20V	2µs

IV. AD633J MEASUREMENTS

The intentions was to measure transfer function of AD633J integrated circuit according to basic multiplying connection and then make conclusions about AD633J frequency parameters, distortion and time delaying of output transfer signal.

It was tried to multiply X signal that was DC voltage valued at 2V with Y bipolar signal valued at ±5V. Firstly, it was harmonic sine wave signal. Secondly, it was triangle signal and the last type was square wave signal with 50% duty cycle.

The expected was corresponding W = ±1V output signal according to equation for transfer function:

$$W = \frac{2.(\pm 5)}{10} = \pm 1 \qquad (5)$$

The output signal was measured for many frequency variations of Y input signals as you can see in the Table 3.

Table 3
Types and Frequency Variations of Y Input Signals

X input	Y input		
DC	SIN	SQUARE	TRIANGLE
	±5V	±5V	±5V
	f (Hz)		
	1	1	1
	10	10	10
	100	100	100
	1k	1k	1k
	10k	3k	10k
	100k	5k	100k
2V	1M	10k	200k
	1.1M	20k	500k
	1.2M	30k	
	1.3M	50k	
	1.4M	70k	
	1.5M	100k	
	1.6M	200k	
	2M	400k	

For illustration there are 3 examples from measurements that prove the multiplying function of analog multiplier. Output waveforms are measured with oscilloscope. Bipolar input signals *Y* are generated by adjustable pulse generator at frequencies of 10Hz.

A. Sine wave waveform measurements

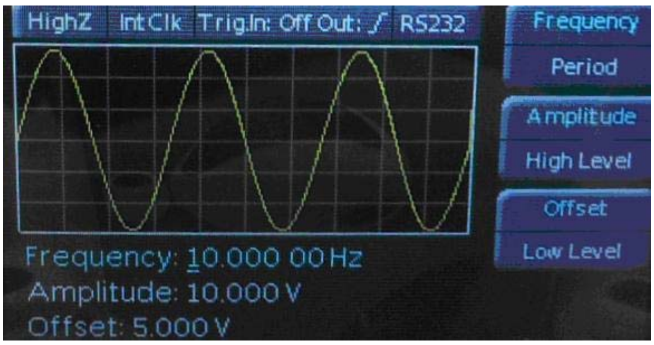


Fig. 4 Sine wave Y input signal, f = 10Hz, U = ±5V

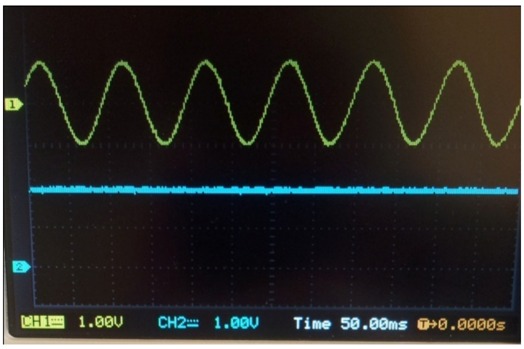


Fig. 5 Output signal of AD633J

B. Square wave waveform measurements

Fig. 6 Square wave Y input signal, f = 10Hz, U = ±5V

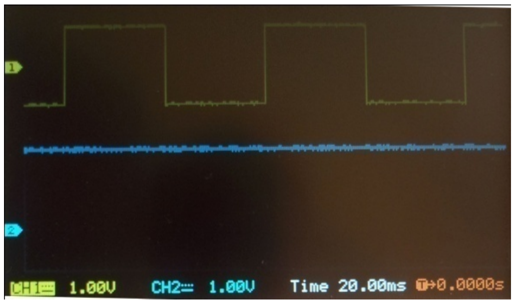


Fig. 7 Output signal of AD633J

C. Triangle wave waveform measurements

Fig. 8 Triangle wave Y input signal, f = 10Hz, U = ±5V

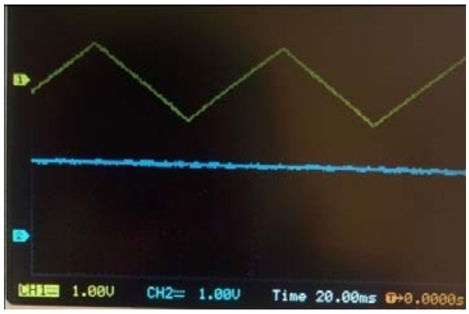


Fig. 9 Output signal of AD633J

D. Time delay of output signal

With frequency increasing, the time delay of output signal from AD633J was noticed. Red-colored values in table 3 are frequencies in which time delay is starting to appear. With the growth of frequency you can see more and more shape distortion. Furthermore, we noticed amplitude distortion mostly when measured sine wave transfer with frequency upper than 1MHz. Some measurements documenting this action are showed in figures Fig. 10 – Fig. 15. Time delay values for certain frequencies are showed in Table 4.

Table 4
Time Delay of Output Transfer Signal

Type of signal	Frequency [Hz]	Time delay [s]
SIN	100k	300n
	1M	300n
SQUARE	50k	200n
	200k	200n
TRIANGLE	200k	200n
	500k	200n

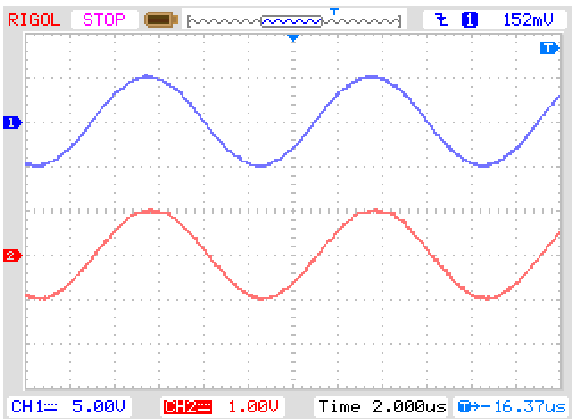


Fig. 10 Sine wave time delay at 100kHz
CH1 - input Y signal ±5V
CH2 - output signal ±1V

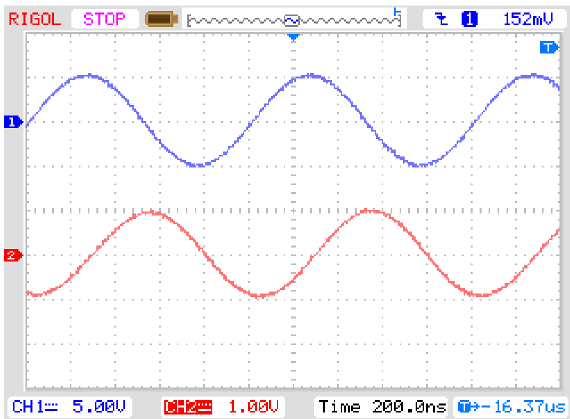


Fig. 11 Sine wave time delay at 1MHz
CH1 - input Y signal ±5V
CH2 - output signal ±1V

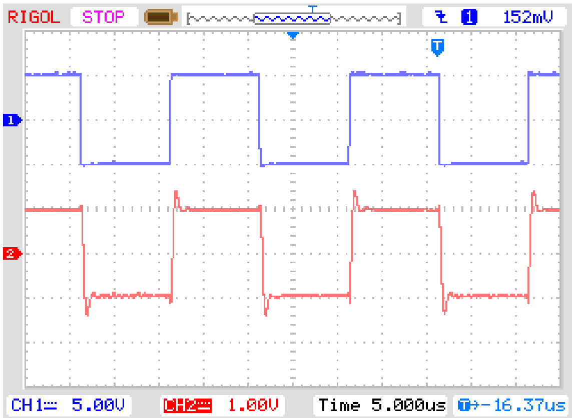


Fig. 12 Square wave time delay at 50kHz
CH1 - input Y signal ±5V
CH2 - output signal ±1V

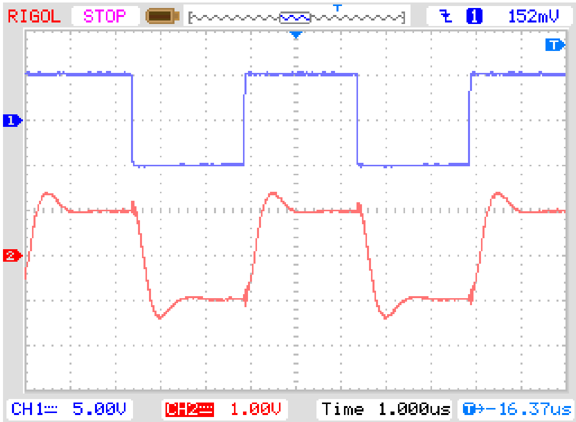


Fig. 13 Square wave time delay at 200kHz
CH1 - input Y signal ±5V
CH2 - output signal ±1V

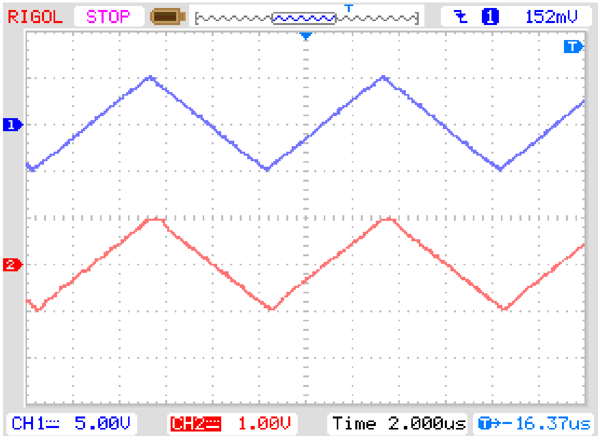


Fig. 14 Triangle wave time delay at 100kHz
CH1 - input Y signal ±5V
CH2 - output signal ±1V

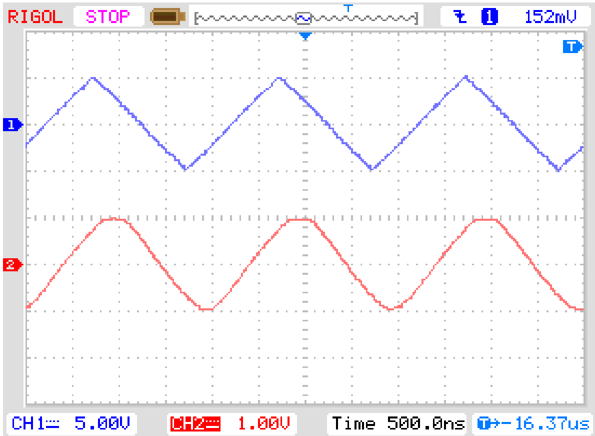
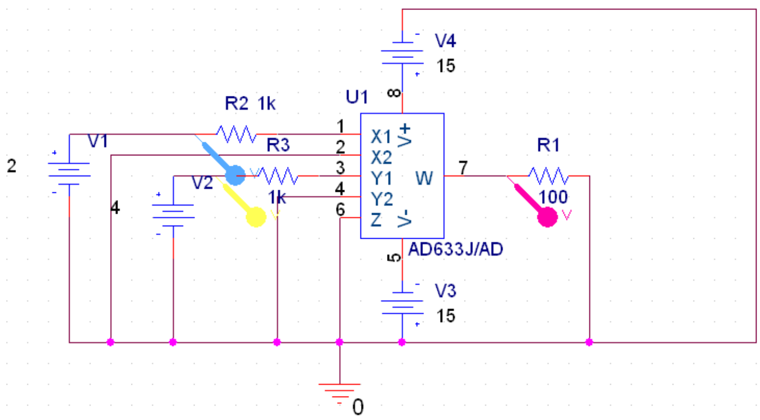


Fig. 15 Triangle wave time delay at 500kHz
CH1 - input Y signal ±5V
CH2 - output signal ±1V

V. PSPICE MODEL OF AD633

To verify the multiplying function of AD633 the software for circuit simulations named Orcad Capture CIS with Pspice was used. AD633J has Pspice model created in *anlg_dev.lib* file. We made simulation with this model and other components in basic application circuit (Fig. 16). It consists of two input DC voltage signals, which are multiplied and the result is output DC voltage via equation for transfer function of AD633:

$$W = \frac{(2-0).(4-0)}{10} + 0 = 0.8 \quad (6)$$



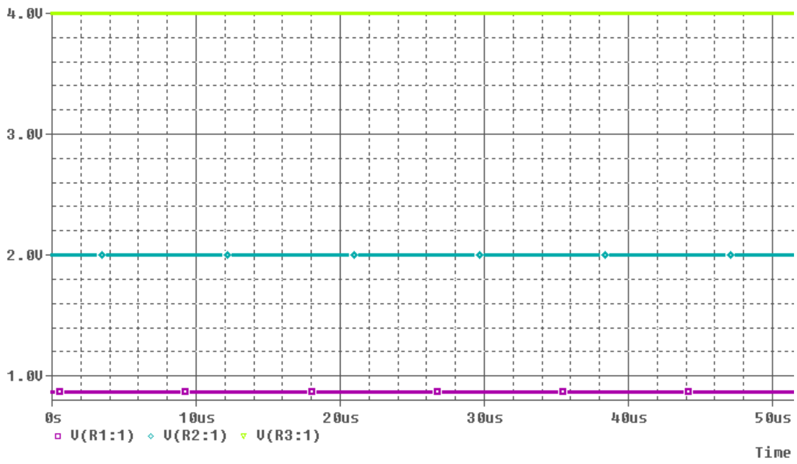


Fig. 16 Schematic and simulation using original Pspice model of AD633J

As is shown, the result of multiplication is right. But, when *Y* input's ideal DC source was changed to pulse source to generate sinus, square or triangle function, the Pspice had problem with convergence of input voltages inside the model. For example sinus source worked only up to frequency of 180 kHz. It was the same with square and triangle, where was supposed that the problem will be with rising edge of input signal. We tried to analyze inner circuit but it was complicated. After redrawing schematic from circuit's netlist we tried to change some values of input RC filters but without success. So, we use easier way - create own pspice model of AD633J.

VI. Creating New Pspice Model Of AD633J

For better simulation results that will correspond to measurements of AD633J we create its new model by adding new sub circuit to *anlg_dev.lib*. We designed new inner structure of AD633J show in picture (17) below.

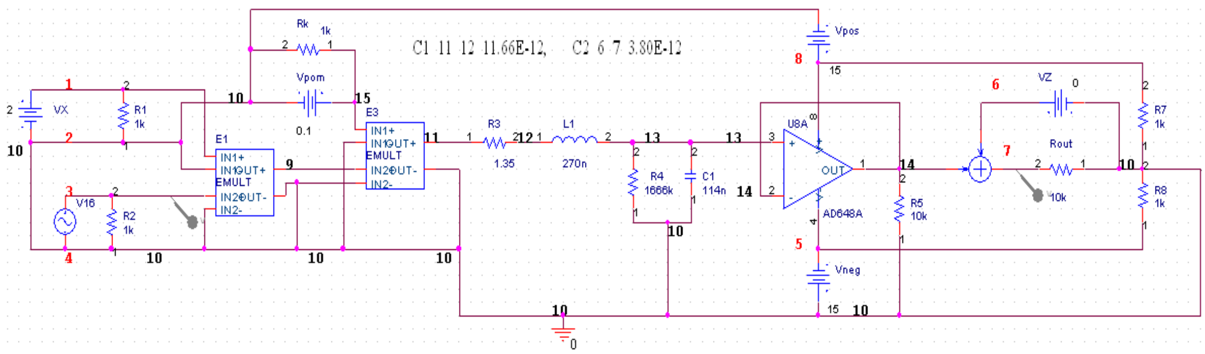


Fig. 17 Schematic of new model of AD633J analog multiplier

Schematic consists of two multiplication cells. The first multiply input *X* and *Y* signals. The second one multiplies the result from first one with constant *k* which is 0.1V. Then the signal is transported through lossless long-distance line that provides time delay. Delayed signal is transported to op-amp connected as emitter follower, where to its output can be added another signal from input *Z* by sum block. In the last step we get the correct result of multiplication, sooner mentioned as *W*. Red numbers represent pins of AD633J integrated circuit. Other components are connected externally to them.

After that we generated the netlist of this circuit and copied it into definition of new sub circuit in *anlg_dev.lib*. We did this in Capture Model Editor. Then the software automatically generated symbol library *anlg_dev.olb* with our new model very simple. The last task was to assign the symbol of AD633J for the OrCad software. We did it with Capture by clicking Edit Symbol after adding component to schematic and redrawing new-generated incorrect symbol with old, more precise graphic symbol [6].

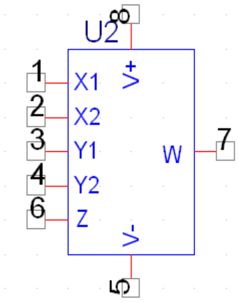


Fig. 18 Model schematic (Fig. 17) hidden in graphic symbol

A. Netlist of new AD633J model

```
* AD633J
* Node assignments
*                        X1  X2  Y1  Y2  V-   Z  W  V+
*                         |   |    |    |    |    |   |    |
.SUBCKT AD633J  1    2    3    4    5    6   7   8
R_R1        1 2  1k
R_R2        3 4  1k
R_R7        8 10 1k
R_R8        10 5 1k
E_E1        9 10 VALUE {V(1,2)*V(3,4)}
E_E3        11 10 VALUE {V(15,10)*V(9,10)}
V_k         15 10 DC 0.1
R_k         15 10 1k
R_R3        11 12  1.35
L_L1        12 13  270n
R_R4        13 10  1666k
C_C1        13 10  114n
X_U8A         13 14 8 5 14 AD648A
R_R5        14 10 10k
E_SUM         7 10 VALUE {V(6,10)+V(14,10)}
R_out       7 10 10k
.ENDS
```

B. Simulation results

In the next few pictures you can find that new simulations also at critical points agree with measured waveforms.

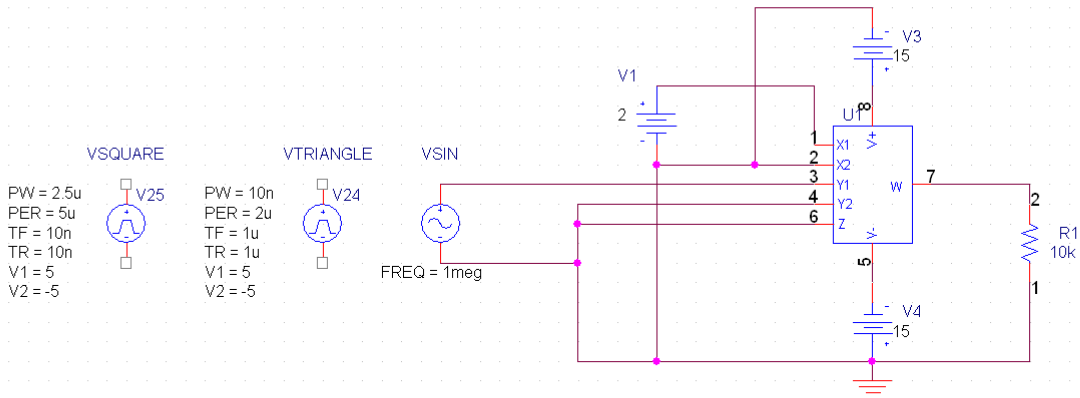


Fig. 19 Schematic of analog multiplier AD633J with various Y input signal, Sine wawe - f = 1MHz, Triangle pulse - f = 500kHz, Square pulse - f = 200kHz

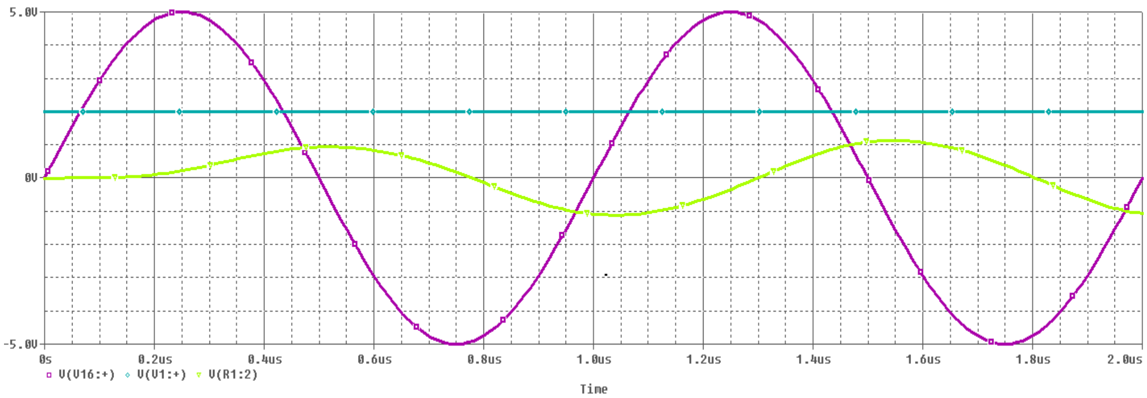


Fig. 20 Simulation results for sine wave Y input; ——— X input DC voltage 2V; ——— Y input sine wave, f = 1MHz; ——— result of multiplication

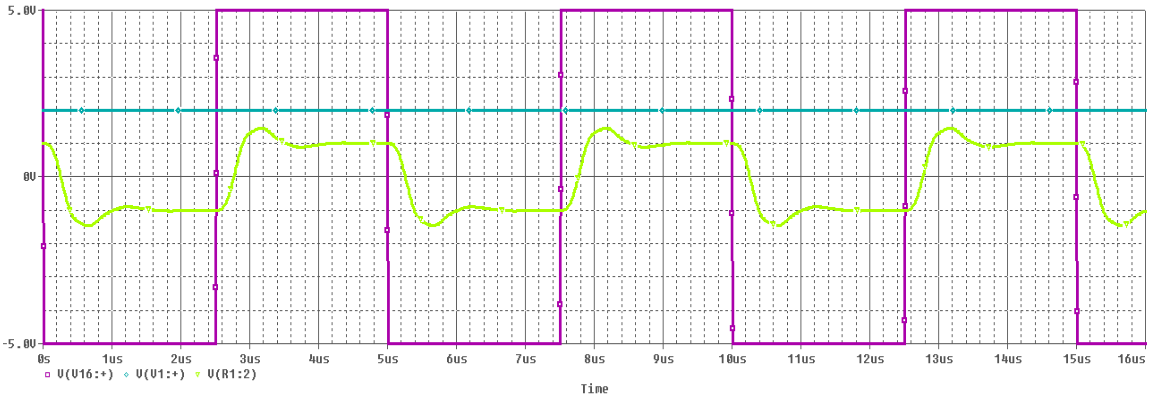


Fig. 21 Simulation results for square pulse Y input, ——— X input DC voltage 2V, ——— Y input sine wave, f = 1MHz, ——— result of multiplication

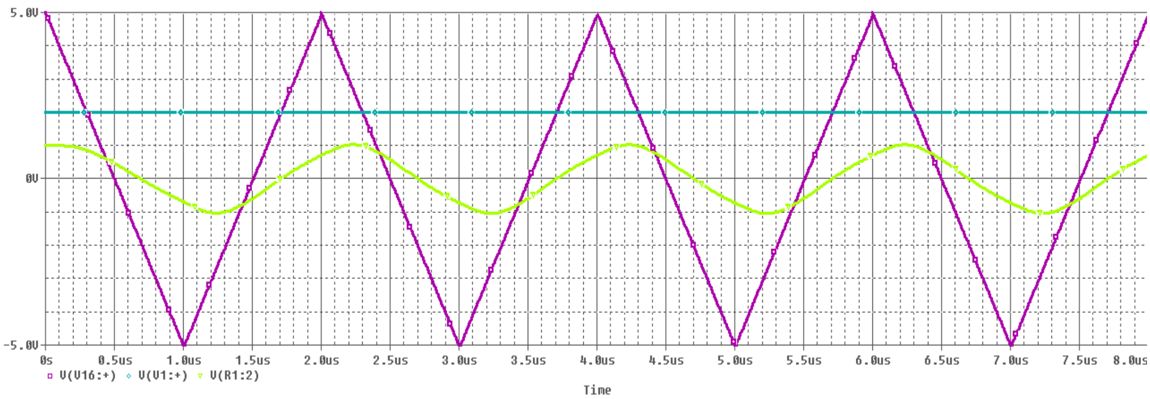


Fig. 22 Simulation results for triangle pulse Y input, ——— X input DC voltage 2V, ——— Y input sine wave, f = 1MHz, ——— result of multiplication

VII. CONCLUSION

The results of designed model of multiplier AD633J confirm good coincidence with real one. Waveforms obtained by simulation and by measurement showing good agreement inside the frequency range from 0 Hz to almost 200 kHz. Such a way the simulation model can be used as low cost and simple replacement for expensive and sensitive real integrated circuit during new circuits developing based on multiplication of two analog signals.

REFERENCES

[1] J. J. Carr , *Linear IC Applications: A Designer's Handbook*, Newnes, 1996, 356 pages
[2] http://pdf.datasheetcatalog.com/datasheet/analogdevices/431190299mlt04.pdf
[3] http://www.analog.com/en/products/linear-products/analog-multipliers-dividers.html
[4] http://www.analog.com/media/en/technical-documentation/data-sheets/AD633.pdf
[5] www.seas.upenn.edu/~jan/spice/PSpice_CaptureGuideOrCAD.pdf